N Channel Field Effect Transistor -Working and Characteristics

FET is three terminal semiconductor devices, with source, drain and gate terminals. In the FET, current flows along a semiconductor path called the *channel*. The FET has a channel consisting of N-type semiconductor (N-channel) or P-type semiconductor (P-channel) material; the gate is made of the opposite semiconductor type. At one end of the channel, there is an electrode called the *source*. At the other end of the channel, there is an electrode called the *drain*. In a JFET, the junction is the boundary between the channel and the gate. Normally, this P-N junction is reverse-biased (a DC voltage is applied to it) so that no current flows between the channel and the gate. When proper voltage is applied between the source and drain, majority carriers in the channel move from source to drain and constitute the drain current. When there is no voltage on the gate, the channel shows its maximum conductance. As the voltage on the gate is more negative, depletion region becomes wider and hence the channel conductivity decreases. Generally the JFETs are called as depletion mode devices.

N- Channel JFET

N channel JFET consists of an n type bar at the sides of which two p type layers are doped. These layers are joined together to form the gate terminal. The source and drain terminals are taken from the other two ends of the bar. In n-channel FET source is connected to the negative pole and drain terminal is connected to the positive pole of the battery V_{DD}. The majority carriers which are electrons in the N-type bar enter the bar through the Source terminal and leave the bar through the Drain terminal. The charge flow is due to flow of electrons from source to drain. This constitute drain current I_D. The gate and source is reverse biased by the battery V_{GG}

The potential difference between source and drain terminals is termed as V_{DS} and potential difference between source and gate terminal is termed as V_{GS}.

Whenever a positive voltage is applied across drain and source terminals, electrons flows from the source 'S' to drain 'D' terminal, where as

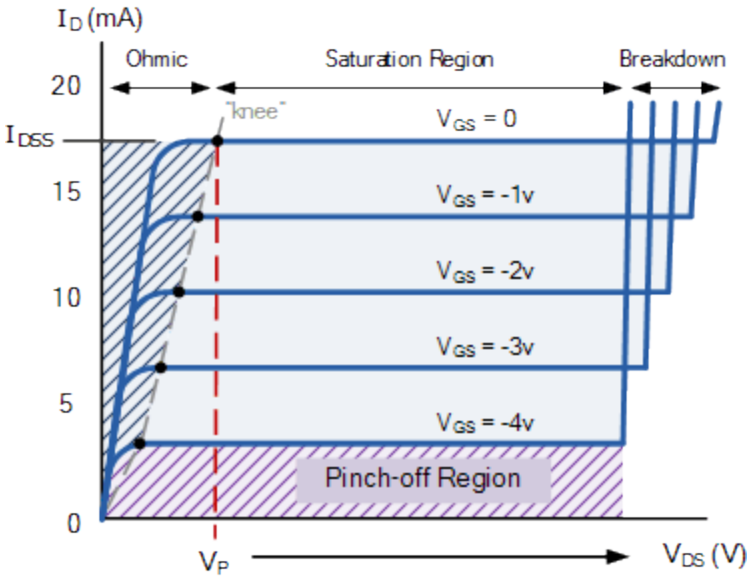
conventional drain current Id flows through the drain to source. As current flows through the device, it is in on state.

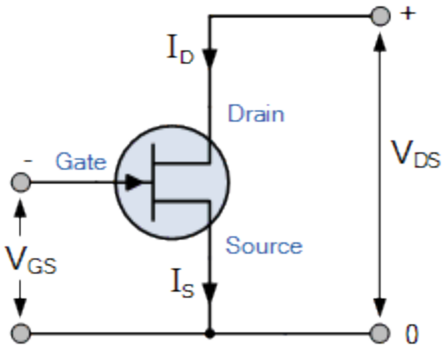
When a negative polarity voltage is applied to the gate terminal, a depletion region is created in the channel. The channel width is reduced, hence increasing the channel resistance between the source and drain. Since the gate source junction is reverse biased and no current flows in the device, it is in off condition.

Characteristics of n- channel Junction FET Transistor

Initially when drain-source voltage V_{DS} and gate-source voltage V_{GS} are zero, there is no attracting potential at the drain, so no current flows. Now the width of depletion region at the gate –channel junction is uniform. This gives drain current $I_D = 0$. For small applied voltage V_{DS}, the N-type bar acts as a simple semiconductor resistor, and the drain current increases linearly with the increase in V_{DS}, up to the knee point. This region, (to the left of the knee point) of the curve is called the channel ohmic *region,* because in this region the FET behaves like an ordinary resistor.

With the increase in drain current I_D, the ohmic voltage drop between the source and channel region reverse-biases the gate junction. The reverse-biasing of the gate junction is not uniform throughout. The reverse bias is more at the drain end than that at the source end of the channel. Therefore the thickness of the depletion region at the drain end is more than at the source end. So with the increase in V_{DS} , the conducting portion of the channel begins to constrict more at the drain end and becomes wedge shaped. Eventually, a voltage V_{DS} is reached at which the channel width is minimum at the drain junction. At this voltage channel is said to be pinched off. The drain current I_D no longer increases with the increase in V_{DS} . It approaches a constant saturation value. The value of voltage V_{DS} at





which the channel is pinched off (i.e. all the free charges from the channel get removed), is called the *pinch-off voltage* V_p. Beyond *pinch-off voltage* V_p the drain current I_D attains a constant value. The region of the characteristic in which drain current I_D remains fairly constant is called *the pinch-off region.* It is also sometimes called the *saturation region* or *amplifier region.* In this region the JFET operates as a *constant current device since* drain current (or output current) remains almost constant. It is the normal operating region of the JFET when used as an amplifier. The drain current in the pinch-off region with $V_{GS} = 0$ is referred to I_{DSS}

If the drain-source voltage, V_{DS} is continuously increased, a stage comes when the gate-channel junction breaks down. At this point current increases

very rapidly and the JFET may be destroyed. This happens because the charge carriers making up the saturation current at the gate channel junction accelerate to a high velocity and produce an *avalanche effect.*

It is also noted that the drain current decreases with the increase in negative gate-source bias.

The drain current I_D flowing through the channel is zero when applied voltage V_{GS} is equal to pinch-off voltage V_P. In normal operation of JFET the applied gate voltage V_{GS} is in between 0 and V_P, In this case the drain current I_D flowing through the channel can be calculated as follows.

$$I_D = I_{DSS} (1-(V_{GS}/V_P))^2$$

Where

I_D = Drain current

I_{DSS} = maximum saturation current

V_{GS} = gate to source voltage

V_P = pinched-off voltage

The drain-source resistance is equal to the ratio of the rate of change in drain-source voltage and rate of change in drain current.

$$R_{DS} = \Delta V_{DS} / \Delta I_D = 1/g_m$$

Where

R_{DS} = drain-source resistance

V_{DS} = drain to source voltage

I_D = drain current

G_m= Trans-conductance gain

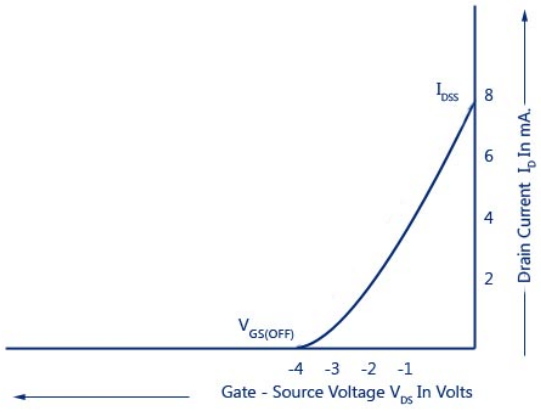
2. *Transfer Characteristic of JFET*

The transfer characteristic is obtained by keeping drain-source voltage, V_{DS} constant and determining drain current, I_D for various values of gate-source voltage, V_{GS}. The curve is plotted between gate-source voltage, V_{GS} and drain current, I_D, as illustrated in fig. It is similar to the transconductance characteristic of a vacuum tube or a transistor. It is observed that

(i) Drain current decreases with the increase in negative gate-source bias

(ii) Drain current, $I_D = I_{DSS}$ when $V_{GS} = 0$

(iii) Drain current, $I_D = 0$ when $V_{GS} = V_{GS\,Off} = V_P$ The transfer characteristic follows equation)



Transfer Characteristics of JFET

BJT	FET
Conduction is due to the flow of both majority & minority charge carriers. Bipolar Device	Conduction is only due to the flow of majority charge carriers. Uunipolar device
Current controlled.device	Voltage controlled.device
Consist of three terminals namely emitter, base and collector.	Consist of three terminals namely source, drain and gate.
The input impedance low compared with FET	The input impedance is high compared with BJT
A BJT needs a small amount of current to switch on the transistor.	Whenever the 'Gate' terminal of the FET transistor has been charged, no more current is required to keep the transistor ON
BJTs are applicable for low current applications	FETS are applicable for low voltage applications.